REMARKS/ARGUMENTS

Claims 1-18 are pending in the application. Claims 1-3, 5-6, 8-10, 12-13, 15, and 17 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Claims 1-3, 5-6, 8-10, 12-13, 15, and 17 have been amended to remove exemplary reference labels. None of these amendments have been made to address any prior-art rejections.

In paragraph 4 of the office action, the Examiner rejected claims 1-3, 5, and 9 under 35 U.S.C. 102(b) as being anticipated by Andoh. In paragraph 6, the Examiner rejected claims 6-7 and 10-11 under 35 U.S.C. 103(a) as being unpatentable over Andoh in view of Hamano. In paragraph 9, the Examiner objected to claims 4, 8, and 12-18 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

Claim 1

Claim 1 is directed to circuitry comprising a first differential transistor pair connected between a first load device and a first current sink. A first inductance-creating element is connected to the first load device to add inductance at a first output node of the circuitry. A power-supply rejection element is connected between the first inductance-creating element and a first voltage reference to provide power-supply rejection at the first output node.

In the non-limiting, exemplary embodiments of Figs. 2-4:

- Transistors M6 and M7 form an example of the first differential transistor pair of claim 1;
- Transistor M4 is an example of the first load device of claim 1;
- Current source I_{total}-I_{neg} is an example of the first current sink of claim 1;
- Transistor M2 is an example of the first inductance-creating element of claim 1;
- VON is an example of the first output node of claim 1;
- Transistor M1 and current source I1 form an example of the power-supply rejection element of claim 1; and
- VDD is an example of the first voltage reference of claim 1.

In rejecting claim 1, the Examiner relied upon Figs. 8 and 9 in Andoh. In particular, the Examiner stated, among other things, that (a) transistor 52 in Andoh's Fig. 9 is an example the first inductance-creating element of claim 1 and (b) transistor 60 in Andoh's Fig. 9 is an example of the power-supply rejection element of claim 1. For the following reasons, the Applicant submits that the Examiner mischaracterized the teachings in Andoh in rejecting claim 1.

First of all, Andoh's transistor 51 is not an inductance-creating element that adds inductance at Andoh's output node 41. Rather, Andoh's transistor 52 is a load device for Andoh's common-mode error amplifier (consisting of transistors 52-60). Significantly, since Andoh's transistor 52 is fed by a common-mode error signal generated by that common-mode error amplifier, it cannot possibly add inductance at output node 41.

Secondly, Andoh's transistor 60 is not a power-supply rejection element. Rather, transistor 60 helps with common-mode rejection, not with power-supply rejection.

For at least these two reasons, the Applicant submits that the Examiner mischaracterized the teachings in Andoh. As such, the Applicant submits that the rejection of claim 1 based on Andoh is improper. None of the other cited references teaches the features in claim 1 that are missing from Andoh.

The Applicant submits therefore that claim 1 is allowable over Andoh and the rest of the cited references. Since the rest of the claims depend variously from claim 1, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

Claim 2

According to claim 2, a second load device is connected to the first differential transistor pair, and a second inductance-creating element is connected to the second load device to add inductance at a second output node of the circuitry, where the power-supply rejection element is connected between the second inductance-creating element and the first voltage reference to provide power-supply rejection at the second output node.

In the non-limiting, exemplary embodiments of Figs. 2-4:

- o Transistor M5 is an example of the second load device of claim 2;
- o Transistor M3 is an example of the second inductance-creating element of claim 2; and
- o VOP is an example of the second output node of claim 2.

In rejecting claim 2, the Examiner also relied upon Figs. 8 and 9 in Andoh. In particular, the Examiner stated, among other things, that transistor 53 in Andoh's Fig. 9 is an example the second inductance-creating element of claim 2. For the following reasons, the Applicant submits that the Examiner also mischaracterized the teachings in Andoh in rejecting claim 2.

Similar to transistor 52, Andoh's transistor 53 is not an inductance-creating element that adds inductance at Andoh's output node 40. Rather, like transistor 52, Andoh's transistor 53 is a load device for Andoh's common-mode error amplifier. Significantly, since Andoh's transistor 53 is fed by a common-mode error signal generated by that common-mode error amplifier, it cannot possibly add inductance at output node 40.

For at least this reason, the Applicant submits that the Examiner further mischaracterized the teaching in Andoh. As such, the Applicant submits that the rejection of claim 2 based on Andoh is also improper. None of the other cited references teaches the features in claim 2 that are missing from Andoh.

The Applicant submits therefore that this provides additional reasons for the allowability of claim 2 (and also claims 3-12, which depend variously from claim 2) over Andoh and the rest of the cited references.

Claim 3

According to claim 3, a second differential transistor pair is connected between the first and second load devices and a second current sink such that the circuitry is adapted to provide a variable-gain amplifier (VGA) function.

In the non-limiting, exemplary embodiments of Figs. 2-3:

- o Transistors M8 and M9 form an example of the second differential transistor pair of claim 3; and
- o Current source I_{neg} is an example of the second current sink of claim 3.

In rejecting claim 3, the Examiner cited Figs. 8 and 9 and column 6, lines 56-63, in Andoh. In particular, the Examiner stated, among other things, that Andoh's circuitry is adapted to provide a VGA function. For the following reasons, the Applicant submits that the Examiner also mischaracterized the teachings in Andoh in rejecting claim 3.

According to column 6, lines 56-63, the gates and drains of transistors 61 and 62 are cross-coupled to each other to improve the Q-factor of the operational transconductance amplifier (OTA). By adjusting control signal $V_{Q\text{-}Control}$, and therefore the current flowing through transistor 63, the output conductance of the OTA can be maximized, and a target gain and frequency response for the OTA may thus be achieved.

This is not a variable-gain amplifier function, as that term is used and understood by those of ordinary skill in the art. Rather, Andoh's transistors 61 and 62 form a negative resistance, tuneable by the control signal, to effectively adjust the Q of a filter, using several copies of the circuitry shown in Fig. 9 as a transconductance amplifier. This is simply not a VGA function.

For at least this reason, the Applicant submits that the Examiner further mischaracterized the teaching in Andoh. As such, the Applicant submits that the rejection of claim 3 based on Andoh is also improper. None of the other cited references teaches the features in claim 3 that are missing from Andoh.

The Applicant submits therefore that this provides additional reasons for the allowability of claim 3 (and also claims 4-8, which depend variously from claim 3) over Andoh and the rest of the cited references.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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